Preferably, an anti-reflection layer **302**, such as a titanium nitride layer, is formed on the metal line **301** before the two layers of the passivation layer.

Referring to FIG. **3B**, an operation of forming a color filter array is carried out to form the color filter **305**. Such operations are known to those of ordinary skill in the art. The color filter **305** may include a red color filter, a green color filter or a blue color filter. The formation of the color filter **305** includes the steps of: a) coating the dyed photoresist **306**; b) performing an exposure and development operation to form the color filter **305** on a light sensing region of the CMOS image sensor; and c) performing a thermal treatment thereafter. As shown in FIG. **3B**, the planarized photoresist **306** is formed on an upper portion of the unit pixel area **300**.

Referring to FIG. **3C**, the micro-lens **307** is formed on the planarized photoresist **306**, and then, a cleaning operation is performed. Referring to FIG. **3D**, the low-temperature oxide layer **308** is coated on the entire structure at a temperature of 150° C. to 200° C. and to a thickness of 3000 Å to 10000 Å.

Referring to FIG. **3E**, after forming the photoresist pattern **309**, the low-temperature oxide layer **308**, the nitride layer **304** and the oxide layer **303** are selectively etched to form the pad open portion **310**. Then, after removing the photoresist pattern **309** and performing a cleaning operation, a package operation is carried out to thereby obtain a CMOS image sensor chip.

Compared with the prior art, since the pad open area formation is carried out after forming the color filter, the planarized photoresist and the micro-lens, it is possible to prevent the surface of the metal line from being damaged or contaminated, thereby improving yield of the CMOS image sensor chip.

Although preferred examples of an apparatus and a method have been disclosed for illustrative purposes, those skilled in the art will appreciate that the scope of this patent is not limited to those examples. On the contrary, the scope of this patent extends to all apparatuses and methods falling within the scope and spirit of the accompanying claims.

What is claimed is:

1. A CMOS image sensor comprising:

a semiconductor structure, wherein the semiconductor structure includes a unit pixel area and a pad area;

a metal line formed on the pad area, wherein a portion of the metal line is exposed;

a passivation layer formed on the unit pixel area and on the metal line such that the exposed portion of the metal line is left exposed;

a planarized photoresist formed on a portion of the passivation layer;

a micro-lens formed on a portion of the planarized photoresist; and

an oxide layer formed on the micro-lens, the photoresist and the passivation layer such that the exposed portion is left exposed.

2. The CMOS image sensor as recited in claim **1**, wherein the oxide layer is formed at a temperature of 150° C. to 200° C.

3. The CMOS image sensor as recited in claim **2**, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

4. The CMOS image sensor as recited in claim **1**, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

5. The CMOS image sensor as recited in claim **1**, wherein the passivation layer includes a nitride layer and a second oxide layer.

6. The CMOS image sensor as recited in claim **4**, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

7. The CMOS image sensor as recited in claim **1**, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

8. A method for fabricating a CMOS image sensor, comprising the steps of:

a) providing a semiconductor structure, wherein the semiconductor structure includes a metal line formed on an upper portion of the semiconductor structure;

b) forming a passivation layer on the metal line;

c) forming a planarized photoresist on a portion of the passivation layer;

d) forming a micro-lens on a portion of the planarized photoresist;

e) forming an oxide layer on the micro-lens, the photoresist and the passivation layer; and

f) forming a pad open mask and etching the oxide layer and the passivation layer to expose a portion of the metal line.

9. The method as recited in claim **8**, wherein the oxide layer is formed at a temperature of 150° C. to 200° C.

10. The method as recited in claim **9**, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

11. The method as recited in claim **8**, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

12. The method as recited in claim **8**, wherein the passivation layer includes a nitride layer and a second oxide layer.

13. The method as recited in claim **12**, further comprising the step of forming an anti-reflection layer on the metal line.

14. The method as recited in claim **13**, wherein the exposed portion of the metal line is not covered by the anti-reflection layer.

15. The method as recited in claim **8**, further comprising the step of forming an anti-reflection layer on the metal line.

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